

Article

A Generalized Multilevel Inverter Based on T-Type Switched Capacitor Module with Reduced Devices

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Abstract: Conventional multilevel inverters have problems in terms of their complicated expansion and large number of devices. This paper proposes a modular expanded multilevel inverter, which can effectively simplify the expansion and reduce the number of devices. The proposed inverter can ensure the voltage balancing of the voltage-dividing capacitors. The cascading of the T-type switched capacitor module and the step-by-step charging method of the switched capacitors enable the inverter to achieve high output voltage levels and voltage gain. In addition, the inversion can be achieved without the H-bridge, which greatly reduces the total standing voltage of the switches. The nine-level inverter of the proposed topology can be realized with only ten switches, obtaining a voltage gain that is two times larger. The above merits were validated through theoretical analysis and experiments. The proposed inverter has good application prospects in medium- and low-voltage photovoltaic power generation.

Keywords: inverter; multilevel inverter; switched capacitor; module; expansion

1. Introduction

The development of solar energy has attracted more and more industry attention in recent years, such as photovoltaic power generation. Power electronics devices are necessary in the process of converting solar energy to electric power. Multilevel inverters (MLIs) have been extensively studied and used because of their advantages of improved power quality, reduced device voltage stress, and reduced filter requirement, etc. [1,2].

Conventional MLIs can be predominantly divided into the following types: neutral-point-clamped (NPC), flying capacitor (FC) and cascade H-bridge (CHB). These inverters have been widely used due to their advantages such as low device voltage stress and low switching frequency [3–5]. Based on the research of conventional MLIs, various new MLIs have been proposed [6]. In order to obtain higher voltage levels than conventional topologies, a new NPC inverter was proposed in [7]. However, the voltage balancing issues of conventional NPC inverters still exist in this NPC inverter. NPC and FC were combined in [8], which increased the output voltage levels. However, at the same time, additional control circuits are required. In [9], the problem of capacitor voltage balancing was solved by replacing the voltage divider capacitors with DC sources. However, multiple DC sources are required, which may limit the device's wide application. Some other studies simplified the inverter control algorithms without affecting the performance. However, the critical problem of voltage balance still exists even if the control algorithm is simplified [10]. Moreover, the mentioned inverters have a common disadvantage in that the expansion is complex and does not have a voltage-boosting ability.

In order to simplify the circuit and reduce the devices, the switched DC source technique is applied to MLIs in [11–13]. However, multiple DC sources are required may limit their applications. The switched capacitor technique provides a good way to solve the limitation of the DC sources because the capacitors used as energy storage elements on the DC side can replace DC sources to supply the load and, at the same time, the voltage gain is obtained. In recent years, switched capacitor multilevel inverters (SCMLIs) have been widely investigated due to their advantages of simple structure and high power density [14,15].

Some single-source SCMLIs were proposed in [16–19]. The number of DC sources is reduced without affecting the voltage gain. Although these inverters have an excellent performance, they also exhibit demerits. The inverter in [16] is well designed so that the working states of the two capacitors are completely synchronized, and the capacitor voltages can be balanced at all times. All switches of the inverter proposed in [17] are contained in two H-bridges, which simplifies the control. However, the above two inverters cannot be expanded. In [18], although an expansion can be achieved by cascading multiple modules, the cascading expansion method will still have the disadvantage of using a large number of DC sources. The expansion method is simplified in [19] with reduced switches. However, the ability to supply inductive loads is not available in this inverter due to the diode's forward bias characteristic. In addition, a common disadvantage of the above four inverters is that an H-bridge composed of four switches that withstand the peak value of the output voltage is used to achieve inversion. This may result in a large total standing voltage (TSV) in the switches.

The H-bridge was eliminated without affecting the voltage polarity conversion in [20,21], and a high voltage gain can be achieved by setting an appropriate DC source ratio. However, multiple DC sources are required, especially when inverters be expanded. In [22,23], the switched capacitor technique was used in NPC inverters, which have the merits of reduced TSV and increased output levels due to the presence of the dividing capacitors. However, the number of devices in the inverter in [22] can be further reduced, and the inverter in [23] cannot be expanded. In [24], a single source inverter without an H-bridge was proposed. The DC source is connected in series with an adjacent capacitor to charge other capacitors, which achieves a high voltage gain. However, the complex expansion may limit its application. In [25,26], the switched capacitor technique is applied to the CHB inverters. By replacing some DC sources with capacitors, the drawback of using multiple DC sources can be effectively solved with the advantage of low voltage stress. However, a large number of switches are required, especially when an expansion is needed. Therefore, their control complexity and capital costs may be increased.

In order to reduce the use of devices and control the complexity, this paper proposes an expandable MLI based on the T-type switched capacitor module (TSCM). Compared to conventional MLIs, the proposed inverter can ensure the voltage balance of voltage-dividing capacitors easily. Moreover, voltage gain that is two times larger can be achieved with a simple expansion capability. Compared to the SCMLIs recently proposed, the proposed inverter eliminates the H-bridge, and can effectively reduce the number of devices. The step-by-step charging method and modular expansion capability enable the inverter to output high voltage levels and achieve high voltage gains with a small number of devices.

2. Proposed Multilevel Inverter

2.1. Circuit Configuration

Figure 1 shows the procedure of developing the multilevel inverters through applying the switched capacitor technique. One disadvantage of conventional multi-level inverters is that they cannot boost the input voltage. The inverters integrating the switched capacitor technique are shown in Figure 2. This type of inverter can obtain a voltage gain. However, the inverters shown in Figure 2a,c use the H-bridge to achieve inversion, which will increase TSV [15,19]. The inverters shown in Figure 2b,d eliminate the H-bridge without affecting the inversion. However, the extension of the

inverter in Figure 2b is complicated [24] and the inverter shown in Figure 2d requires a large number of devices [26].

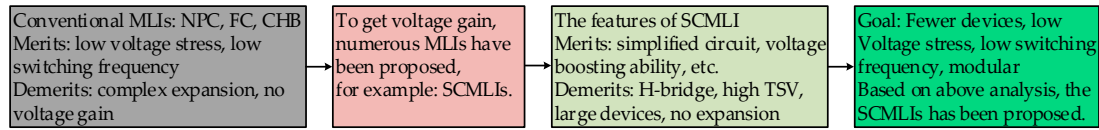


Figure 1. The procedure of developing the multilevel inverter.

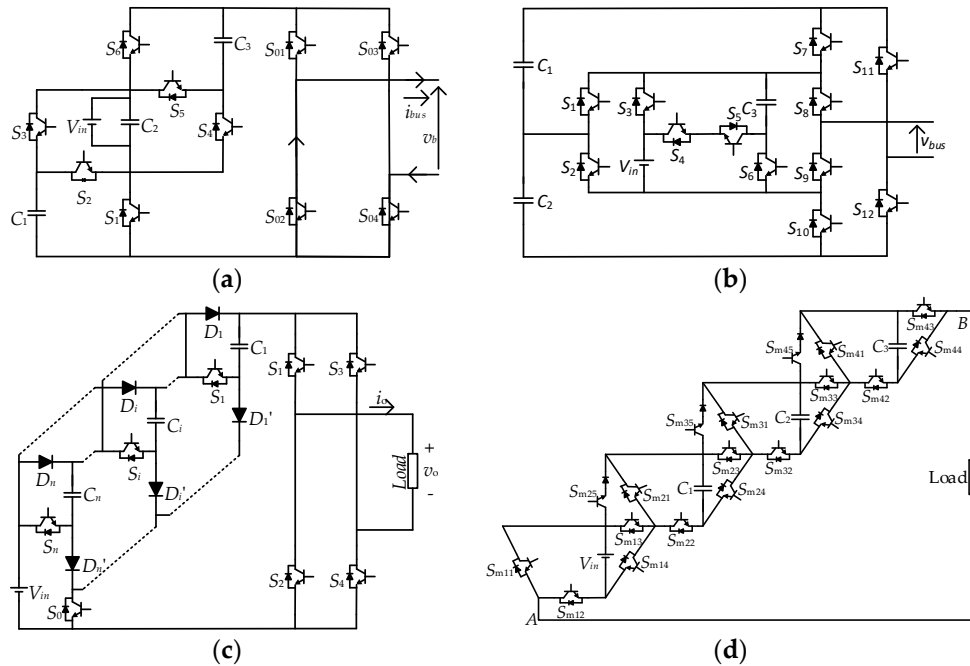


Figure 2. The inverters proposed in open literatures. (a) The inverter proposed in [15]. (b) The inverter proposed in [24]. (c) The inverter proposed in [19]. (d) The inverter proposed in [26].

Based on the above research, an SCMLI is proposed to obtain a voltage gain and reduce the devices with the characteristics of easy expansion and low TSV. The proposed nine-level inverter consists of a DC link, a TSCM and two bridges (L and R), as shown in Figure 3. The DC source in the DC link provides energy for the circuit and the DC link capacitors provide a level of $0.5 V_{dc}$. The voltage boosting capability is obtained by the TSCM, which can be cascaded to get high-level inverters. The output voltage polarity conversion is realized by the L-bridge and R-bridge.

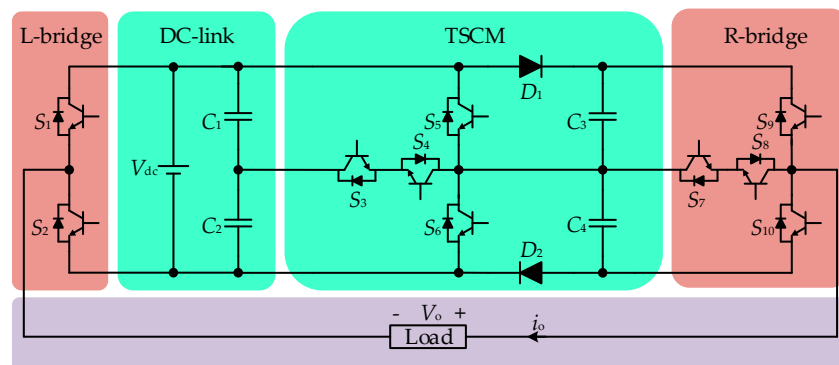


Figure 3. The proposed nine-level inverter.

2.2. Charging Method of Switched Capacitors

As mentioned above, the expansion can be achieved through cascading multiple TSCMs. The capacitors in the former TSCM is connected in series to charge the capacitors in the latter TSCM. The charging process is called the step-by-step charging method, which enables the levels and voltage gain of the expanded inverter to be greatly increased. The principle of the step-by-step charging method is shown in Figure 4.

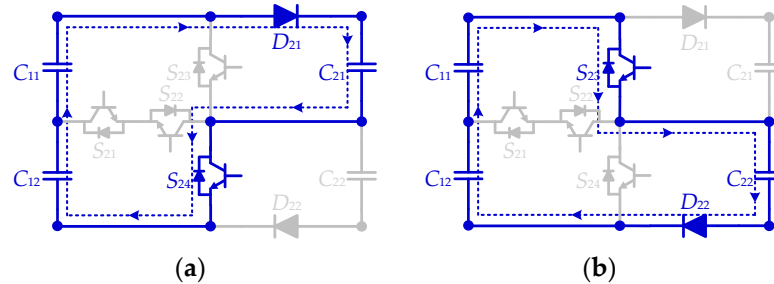


Figure 4. The charging principle of capacitors in the T-type switched capacitor module (TSCM). (a) The charging path of the first capacitor in the TSCM. (b) The charging path of the second capacitor in the TSCM.

2.3. Operating Principle

The inverter can achieve nine different operating modes by controlling the on and off states of each switch: $+2V_{dc}$, $+1.5V_{dc}$, $+V_{dc}$, $+0.5V_{dc}$, 0 , $-0.5V_{dc}$, $-V_{dc}$, $-1.5V_{dc}$, $-2V_{dc}$. The energy paths of the nine working modes are shown in Figure 5a–i. The states of the switches, diodes and capacitors in each mode are shown in Table 1.

Table 1. States of devices in different modes.

V_o	Switches	Diodes		Capacitors			
	$S_1 S_2 S_3 S_4 S_5 S_6 S_7 S_8 S_9 S_{10}$	D_1	D_2	C_1	C_2	C_3	C_4
$+2V_{dc}$	0100100010	0	0	▲	▲	▼	—
$+1.5V_{dc}$	0111000010	0	0	▲	▼	▼	—
$+V_{dc}$	0100010010	1	0	▲	▲	▲	—
$+0.5V_{dc}$	0111001100	0	0	▲	▼	—	—
0	1000101100	0	0	▲	▲	—	—
$-0.5V_{dc}$	1011001100	0	0	▼	▲	—	—
$-V_{dc}$	1000100001	0	1	▲	▲	—	▲
$-1.5V_{dc}$	1011000001	0	0	▼	▲	—	▼
$-2V_{dc}$	1000010001	0	0	▲	▲	—	▼

Note: “1” and “0” in the table are the on and off states of the corresponding devices. “▲”, “▼” and “—” indicate the charging, discharging, and rest states of the capacitors. V_o is the output voltage.

Mode 1 ($V_o = +2V_{dc}$): As shown in Figure 5a, S_2 , S_5 and S_9 are turned on, whereas other switches are turned off. D_1 is reverse biased while D_2 is forward biased. C_3 is discharged in series with the DC source to supply the load, and C_1 , C_2 and C_4 are being charged.

Mode 2 ($V_o = +1.5V_{dc}$): As shown in Figure 5b, S_2 , S_3 , S_4 and S_9 are turned on, whereas other switches are turned off. D_1 and D_2 are reverse biased. C_2 and C_3 are discharged in series to supply the load, and C_1 is being charged while C_4 rests.

Mode 3 ($V_o = +V_{dc}$): As shown in Figure 5c, S_2 , S_6 and S_9 are turned on, whereas other switches are turned off. D_1 is forward biased and D_2 is reverse biased. C_1 , C_2 and C_3 are being charged while C_4 rests, and the dc source alone supplies the load.

Mode 4 ($V_o = +0.5V_{dc}$): As shown in Figure 5d, S_2 , S_3 , S_4 , S_7 and S_8 are turned on, whereas other switches are turned off. D_1 and D_2 are reverse biased. C_2 is discharged to supply the load, and C_1 is being charged while C_3 and C_4 rest.

Mode 5 ($V_o = 0$): As shown in Figure 5e, S_1 , S_5 , S_7 and S_8 are turned on, whereas other switches are turned off. D_1 is reverse biased while D_2 is forward biased. C_1 and C_2 are being charged while C_3 and C_4 rest.

Mode 6 ($V_o = -0.5V_{dc}$): As shown in Figure 5f, S_1 , S_3 , S_4 , S_7 and S_8 are turned on, whereas other switches are turned off. D_1 and D_2 are reverse biased. C_1 is discharged to supply the load, and C_2 is being charged while C_3 and C_4 rest.

Mode 7 ($V_o = -V_{dc}$): As shown in Figure 5g, S_1 , S_5 and S_{10} are turned on, whereas other switches are turned off. D_1 is reverse biased and D_2 is forward biased. C_1 , C_2 and C_4 are being charged while C_3 rests, and only the dc source supplies the load.

Mode 8 ($V_o = -1.5V_{dc}$): As shown in Figure 5h, S_1 , S_3 , S_4 and S_{10} are turned on, whereas other switches are turned off. D_1 and D_2 are reverse biased. C_1 and C_4 are discharged in series to supply the load, and C_2 is being charged while C_3 rests.

Mode 9 ($V_o = -2V_{dc}$): As shown in Figure 5i, S_1 , S_6 and S_{10} are turned on, whereas other switches are turned off. D_1 is forward biased while D_2 is reverse biased. C_4 is discharged in series with the DC source to supply the load, and the capacitors C_1 , C_2 and C_3 are being charged.

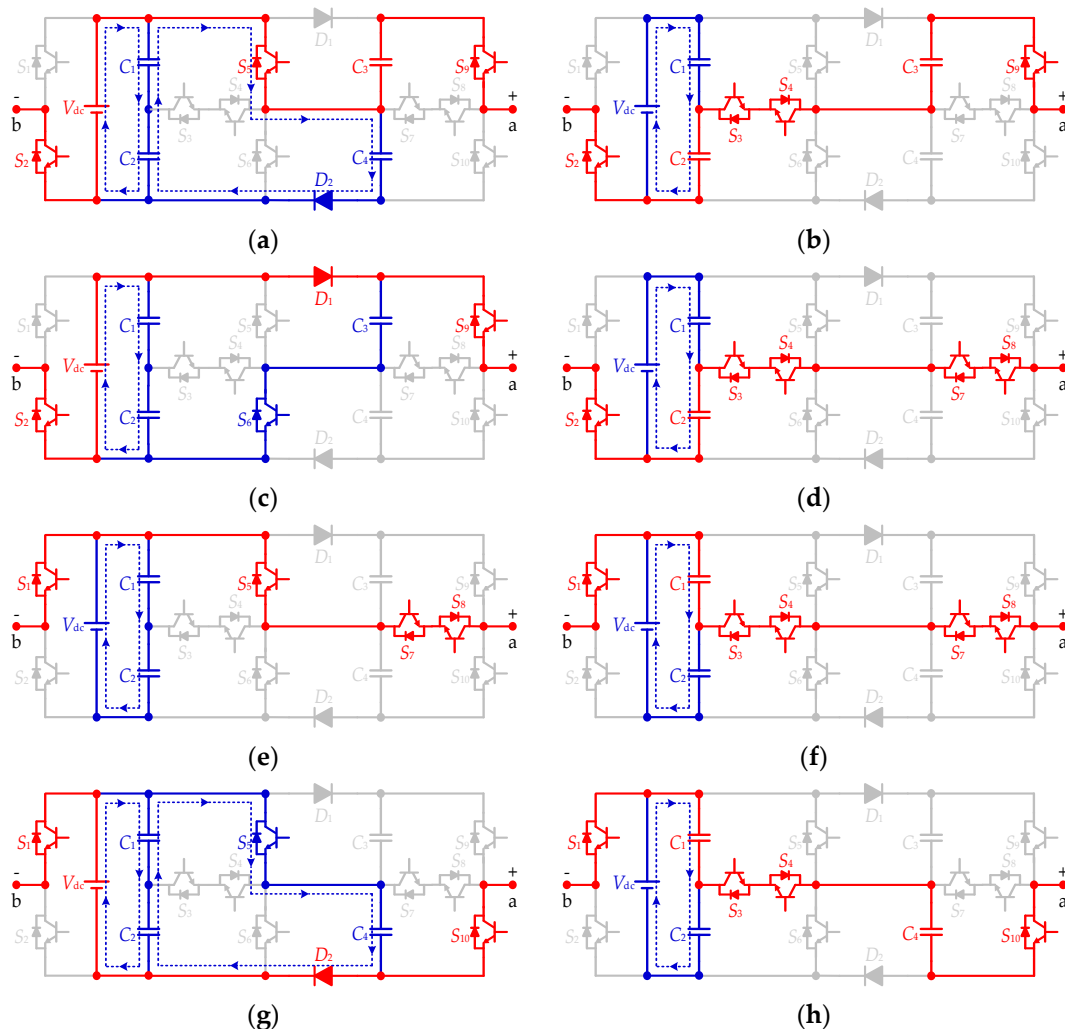


Figure 5. Cont.

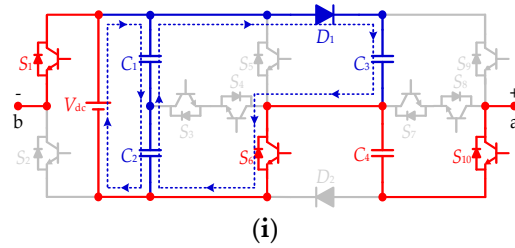


Figure 5. Operating modes. (a) $+2V_{dc}$, (b) $+1.5V_{dc}$, (c) $+V_{dc}$, (d) $+0.5V_{dc}$, (e) 0, (f) $-0.5V_{dc}$, (g) $-V_{dc}$, (h) $-1.5V_{dc}$, (i) $-2V_{dc}$.

The red lines in Figure 5 show that the capacitors and sources are supplying the load, and the blue lines show the capacitors are being charged by the DC source. In addition, energy has forward and reverse paths in each mode, proving that the inverter has the ability to integrate inductive loads.

2.4. Modulation Strategy

The pulse width modulation (PWM) is mainly divided into three types: carrier wave PWM, eliminating the specific harmonics PWM (SHEPWM) and space vector PWM (SVPWM). The SVPWM method is suitable for inverters which output three to five levels. However, it is not suitable when inverters output more than five levels due to its complexity [27]. The ladder wave equal PWM (EPWM) method is one method of carrier wave PWM. The advantage of this method is that the conduction angle is selective to eliminate certain order harmonics, which is beneficial in reducing the output voltage THD. Another advantage is that it can effectively reduce the switching frequency [28].

To make the output waveform of the inverter approximate to a sinusoidal wave, a nine-level inverter is selected as a showcase, as shown in Figure 6. Based on the superposition principle, a nine-level staircase wave can be formed by four rectangular waves V_{oi} ($i = 1, 2, 3, 4$) with the same amplitude and frequency. Assuming that the amplitude of the sine wave is $2V_{dc}$, the amplitude of V_{oi} can be divided into four to obtain an amplitude of $0.5V_{dc}$, and the frequency is the same as the output fundamental wave f_o .

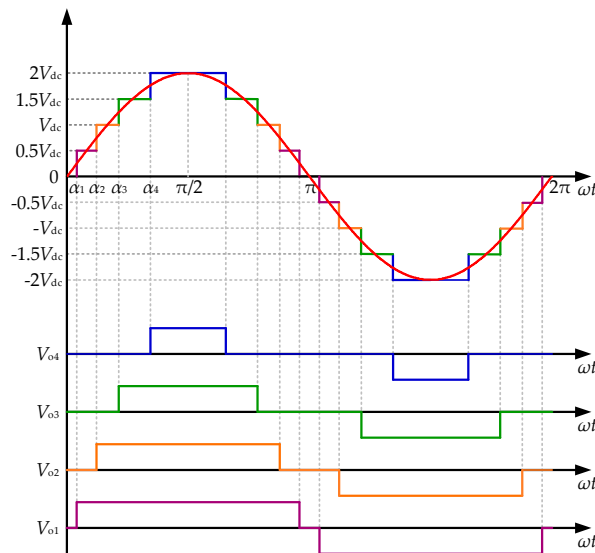


Figure 6. Schematic diagram of the ladder wave equal pulse width modulation (EPWM).

In Figure 6, α_i ($i = 1, 2, 3, 4, \alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \pi/2$) is the initial conducting angle of the rectangular wave. The values of these four angles affect the time width of the rectangular wave and, therefore, the quality of the inverter output waveform. The Fourier decomposition of rectangular wave V_{oi} is:

$$V_{oi} = \frac{2V_{dc}}{\pi} \sum_{k=1,3,\dots}^{\infty} \frac{\cos(k\alpha_i)}{k} \sin(k\omega t) \quad (1)$$

where ω is the fundamental angular frequency of the output waveform.

Therefore, the output voltage V_o can be expressed as (2), because the nine-level staircase wave is formed by the superposition of the four rectangular waves.

$$V_o = \frac{2V_{dc}}{\pi} \sum_{k=1,3,\dots}^{\infty} \sum_{i=1}^4 \frac{\cos(k\alpha_i)}{k} \sin(k\omega t) \quad (2)$$

then, the fundamental wave modulation index M is:

$$M = \frac{1}{4} \sum_{i=1}^4 \cos \alpha_i \quad (3)$$

The definition of the THD of the output voltage is:

$$\text{THD} = \sqrt{\frac{\sum_{k=2}^{\infty} V_k^2}{V_1^2}} \times 100\% \quad (4)$$

Combing (2) and (4), the THD of the output nine-level staircase wave is:

$$\text{THD} = \sqrt{\frac{\sum_{k=3,5,\dots}^{\infty} \left[\sum_{i=1}^4 \frac{\cos(k\alpha_i)}{k} \right]^2}{\sum_{i=1}^4 \alpha_i}} \times 100\% \quad (5)$$

It can be seen from (5) that the conducting angle α_i is the only variable that affects the output voltage THD. Therefore, selecting a proper α_i is the main target of the modulation analysis when the fundamental wave modulation index M has been determined. It is easy to determine the initial value of the conducting angle according to the equal area rule of the waveform approximation method [27]. However, some low-order harmonics are the dominating components of the total harmonics in the output voltage. Another way to obtain the initial value of the conducting angle is to set up simultaneous equations which conclude with the conducting angle α_i . Before this, the order of the harmonics to be eliminated should be selected. The third harmonic is automatically eliminated in a three-phase system [28]. The $6j \pm 1$ ($j = 1, 2, 3, \dots$) harmonics are the main elements to be eliminated. Therefore, for a nine-level inverter, only the first three third-order harmonics (5th, 7th, and 11th), which are the dominating harmonics, will be eliminated through the modulation. The conducting angles can be determined according to (6).

$$\begin{cases} \cos \alpha_1 + \cos \alpha_2 + \cos \alpha_3 + \cos \alpha_4 = 4M \\ \cos 5\alpha_1 + \cos 5\alpha_2 + \cos 5\alpha_3 + \cos 5\alpha_4 = 0 \\ \cos 7\alpha_1 + \cos 7\alpha_2 + \cos 7\alpha_3 + \cos 7\alpha_4 = 0 \\ \cos 11\alpha_1 + \cos 11\alpha_2 + \cos 11\alpha_3 + \cos 11\alpha_4 = 0 \end{cases} \quad (6)$$

3. Capacitor Analysis and Loss Calculation

3.1. Capacitor Calculation

As the capacitors $C_1 + C_4$ and $C_2 + C_3$ operate as two switching pairs, only C_2 and C_3 are analyzed as an example. It can be seen from Figure 5 and Table 1 that C_2 is discharged when the output voltage is $+0.5V_{dc}$ and $+1.5V_{dc}$, and C_3 is discharged when the output voltage is $+1.5V_{dc}$ and $+2V_{dc}$. In order to obtain the maximum discharge amount, the parasitic parameters of each component are not considered in the discharging loops of the capacitors.

The discharge amount of C_2 in the interval of $+0.5 V_{dc}$ [α_1, α_2] is:

$$\Delta Q_{C2_0.5} = \frac{1}{2\pi f_o} \int_{\alpha_1}^{\alpha_2} \frac{V_{dc}}{2R} d\omega t \quad (7)$$

where $\Delta Q_{C2_0.5}$ is the discharge amount of C_2 in [α_1, α_2], R is the load, f_o is the fundamental frequency, and ω is the fundamental angular frequency. Further calculations can be given as:

$$\Delta Q_{C2_0.5} = \frac{V_{dc}(\alpha_2 - \alpha_1)}{2\pi f_o R} \quad (8)$$

In the same way, the discharge amount ($\Delta Q_{C2_1.5}$) of C_2 in the interval [α_3, α_4] when the output voltage is $+1.5V_{dc}$ is:

$$\Delta Q_{C2_1.5} = \frac{3V_{dc}(\alpha_4 - \alpha_3)}{2\pi f_o R} \quad (9)$$

The continuous working interval of C_3 is [$\alpha_3, \pi - \alpha_3$]; the discharge amount of C_3 in this interval is:

$$\Delta Q_{C3} = \frac{1}{2\pi f_o} \left[\int_{\alpha_3}^{\alpha_4} \frac{3V_{dc}}{2R} d\omega t + \int_{\alpha_4}^{\pi - \alpha_4} \frac{2V_{dc}}{R} d\omega t + \int_{\pi - \alpha_4}^{\pi - \alpha_3} \frac{3V_{dc}}{2R} d\omega t \right] \quad (10)$$

the variables involved in (10) are the same as those in (7). Further calculations show that the discharge amount of C_3 is:

$$\Delta Q_{C3} = \frac{V_{dc}(2\pi - 3\alpha_3 - \alpha_4)}{2\pi f_o R} \quad (11)$$

The voltage ripple of the capacitor is inversely proportional to the capacitance. Assuming that the voltage ripple of the capacitor does not exceed 10% of the set value of the capacitor, the maximum capacitor voltage ripple can be accepted as $0.1V_C$ (V_C is the voltage of the capacitor). The minimum capacitance is:

$$C_{1min} = C_{2min} = \frac{\Delta Q_{C2_1.5}}{0.1V_{dc}} = \frac{15(\alpha_4 - \alpha_3)}{\pi f_o R} \quad (12)$$

$$C_{3min} = C_{4min} = \frac{\Delta Q_{C3}}{0.1V_{dc}} = \frac{10\pi - 15\alpha_3 - \alpha_4}{\pi f_o R} \quad (13)$$

It should be mentioned that the reason for choosing $\Delta Q_{C2_1.5}$ as the discharge amount of C_2 in (12) is that $\Delta Q_{C2_1.5}$ is the maximum continuous discharge amount of C_2 . It can be seen from (12) and (13) that the capacitance is inversely proportional to the load, voltage ripple, and output frequency. Figure 7 is the voltage of C_3 under different capacitances. As shown in Figure 7 and (14)–(16), increasing the capacitance is beneficial to reduce the voltage ripple. To enhance the performance of the inverter, the capacitance would be better to be appropriately increased when the voltage ripple condition can be met. In this way, the voltage ripple can be reduced and the lifetime of the capacitors can be prolonged.

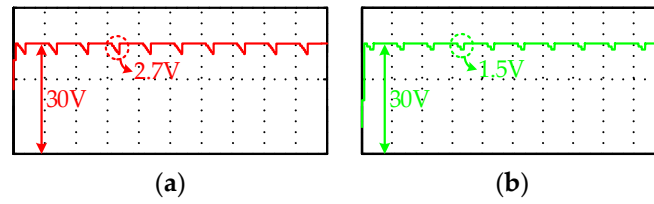


Figure 7. Comparison of voltage ripple under different capacitance. (a) The capacitance is 2200 μF . (b) The capacitance is 4700 μF .

3.2. Analysis of Voltage Balance

As shown in Figure 8, the voltage-dividing capacitors have symmetrical working states in the positive and negative half cycles of the inverter by using the appropriate modulation method. Capacitor voltages vary around their set values. The sum of the voltages of the two capacitors is 30 V, which can always be maintained at a constant value. Each of the T-type switched capacitors works in the half cycle, and their working states do not affect each other. Therefore, the two capacitors are balanced within one cycle. This conclusion can also be drawn from the experimental results in Figure 17b.

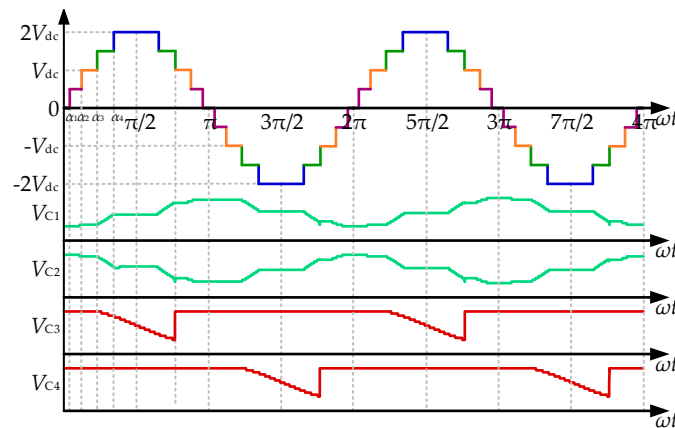


Figure 8. The capacitor working state curve within two cycles.

3.3. Loss Calculations

This section analyzes the various losses of the inverter, including the ripple losses of capacitors (P_{rip}), conduction losses (P_{con}) and switching losses (P_{sw}).

P_{rip} is caused by the voltage fluctuation of the capacitors. This section still takes C_2 and C_3 as examples, because of their symmetrical working states. C_2 is discharged at the output voltages of $0.5V_{\text{dc}}$ and $1.5V_{\text{dc}}$. With the capacitance value determined, the voltage ripples of the two working modes are:

$$\Delta V_{C2_{0.5}} = \frac{\Delta Q_{C2_{0.5}}}{C_2} = \frac{V_{\text{dc}}(\alpha_2 - \alpha_1)}{2\pi f_0 R C_2} \quad (14)$$

$$\Delta V_{C2_{1.5}} = \frac{\Delta Q_{C2_{1.5}}}{C_2} = \frac{3V_{\text{dc}}(\alpha_4 - \alpha_3)}{2\pi f_0 R C_2} \quad (15)$$

Similarly, the voltage ripple of C_3 is:

$$\Delta V_{C3} = \frac{\Delta Q_{C3}}{C_3} = \frac{V_{\text{dc}}(2\pi - 3\alpha_3 - \alpha_4)}{2\pi f_0 R C_3} \quad (16)$$

Therefore, P_{rip} can be calculated as:

$$P_{\text{rip}} = f_0 [2C_2(\Delta V_{C2_{0.5}}^2 + \Delta V_{C2_{1.5}}^2) + C_3 \Delta V_{C3}^2] \quad (17)$$

P_{con} is caused by the parasitic parameters of the circuit elements, such as the voltage drop and the on-state resistance of the diodes and switches, and the parasitic resistance of the capacitors. Taking the positive half cycle as an example for analysis, the equivalent circuits of the four working modes of the positive half cycle are shown in Figure 9.

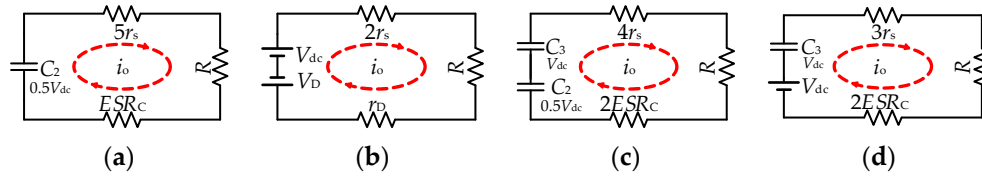


Figure 9. Equivalent circuits of four working modes. (a) $+0.5V_{dc}$, (b) $+V_{dc}$, (c) $+1.5V_{dc}$, (d) $+2V_{dc}$.

The parameters of each component are as follows: V_D and R_D are the voltage drop and on-state resistance of the diode, ESR_C and r_s are the equivalent resistance of the capacitor and the switch, R is the load, and i_o is the output current. The equivalent parameters of the components in the four working modes of the positive half cycle are shown in Table 2. The value of i in Table 2 indicates that the output voltage V_o is i multiplied by $0.5V_{dc}$, and V_{eq} and r_{eq} are the equivalent parasitic resistance and equivalent output voltage.

Table 2. Equivalent parameters of each mode.

i	V_{eq}	r_{eq}
1	$0.5V_{dc}$	$5r_s + ESR_C$
2	$V_{dc} - V_D$	$2r_s + r_D$
3	$1.5V_{dc}$	$4r_s + 2ESR_C$
4	$2V_{dc}$	$3r_s + ESR_C$

Therefore, P_{con} can be calculated as:

$$P_{\text{con}} = \frac{2}{\pi} \sum_{i=1}^4 \left[\left(\frac{V_{eq}}{R + r_{eq}} \right)^2 \times r_{eq} \times (\alpha_{i+1} - \alpha_i) \right] \quad (18)$$

where α_i is the conducting angle, which can be calculated from (6), and the value of α_5 is $\pi/2$.

P_{sw} is caused by a non-abrupt change in voltage and current, which is related to the voltage stress and the operating frequency of the switches, and can be estimated based on the charging and discharging of the switch parasitic capacitance C_{ds} [16]. Table 3 shows the frequency and voltage stress of each switch in the nine-level inverter, where f_s and V_s are the operating frequency and voltage stress of the switches.

Table 3. Voltage stress and frequency of switches.

Switches	S_{1-2}	S_{3-4}	S_5	S_{6-8}	S_{9-10}
f_s	f_o	$8f_o$	$5f_o$	$2f_o$	f_o
V_s	V_{dc}	$0.5V_{dc}$	V_{dc}	V_{dc}	$2V_{dc}$

According to the calculation method in [16], the losses of the switches can be expressed as:

$$P_{\text{sw}} = f_s C_{ds} V_s^2 \quad (19)$$

therefore, the total losses of the switches are:

$$P_{\text{sw}} = 25f_o C_{ds} V_{dc}^2 \quad (20)$$

In summary, the efficiency of the nine-level inverter can be calculated as:

$$\eta = \frac{P_o}{P_o + P_{rip} + P_{con} + P_{sw}} \quad (21)$$

where η and P_o are the efficiency and output power of the proposed nine-level inverter.

4. Analysis of Expansion and Comparison

4.1. Cascaded Topology of Multi-TSCM

The expansion can be achieved by cascading multiple TSCMs without adding additional devices, which is simple to operate and easy to modularize. The expansion topology is shown in Figure 10.

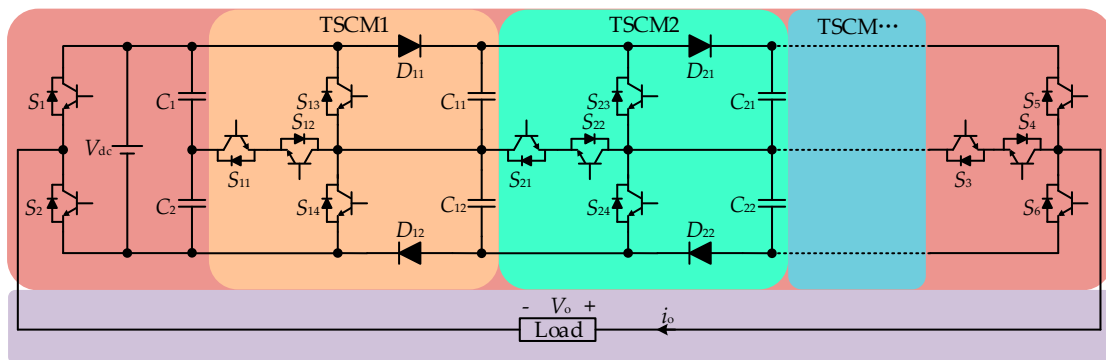


Figure 10. Cascaded topology of multi-TSCM.

As mentioned above, the output levels and voltage gain are greatly improved due to the use of the step-by-step charging method. The relationships between the output levels N and voltage gain G and the number of modules x are:

$$N = 2^{x+2} + 1 \quad (22)$$

$$G = 2^x \quad (23)$$

It can be seen from (22) and (23) that the output levels and voltage gain increase exponentially with the number of modules, which indicate that the output levels and voltage gain of the inverter will increase rapidly with the increase in the TSCMs. The growth curves are shown in Figure 11.

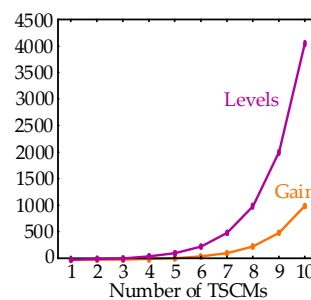


Figure 11. Growth curves of output levels and voltage gain.

Taking the extended inverter with two cascaded TSCMs as an example to analyze its working modes, in this case, the inverter can achieve a 17-level output and a voltage gain that is four times larger. Table 4 shows the working states of the devices in each working mode of the positive half cycle. The definitions of numbers and symbols in Table 4 are the same as those in Table 1.

Table 4. Working state of devices in the 17-level inverter.

V_o	Switches	Diodes	Capacitors
	$S_1 S_2 S_{11} S_{12} S_{13} S_{14} S_{21} S_{22} S_{23} S_{24} S_3 S_4 S_5 S_6$	$D_{11} D_{12} D_{13} D_{14}$	$C_1 C_2 C_{11} C_{12} C_{21} C_{22}$
$+4V_{dc}$	01001000100010	0101	▲▲▼▼▲▲
$+3.5V_{dc}$	01110000100010	0000	▲▼▼—▼—
$+3V_{dc}$	01000100100010	0100	▲▲—▲▼—
$+2.5V_{dc}$	01110011000010	0000	▲▼—▼—
$+2V_{dc}$	01000111010010	0100	▲▲—▲▼—
$+1.5V_{dc}$	01110000010010	0010	▲▼▼—▲—
$+1V_{dc}$	01000100010010	0101	▲▲▲—▲—
$+0.5V_{dc}$	01110011001100	0000	▲▼—
0	10001011001100	0100	▲▲—▲—

4.2. Comparisons with Other Inverters

In order to compare the performance of the inverters, the proposed nine-level inverter is compared with the recently proposed excellent topologies in terms of voltage gain, number of switches, TSV and expansion ability. The results are shown in Table 5.

Table 5. Comparison with different switched capacitor multilevel inverters (SCMLIs).

Items	[15]	[19]	[23]	[24]	[26]	Proposed
Gain	4	4	no	4	4	2
Switches	13	8	12	12	19	10
Capacitors	3	3	4	3	3	4
TSV	$25V_{dc}$	$32V_{dc}$	$6V_{dc}$	$24V_{dc}$	$19V_{dc}$	$11V_{dc}$
H-bridge	yes	yes	no	no	no	no
Inductive load ability	yes	no	yes	yes	yes	yes
Expanded ability	yes	yes	no	yes	yes	yes

It can be seen from Table 5 that the proposed topology shows advantages in terms of the number of switches and TSV. The voltage gain is half of other inverters. This is because that there are two voltage-dividing capacitors in the DC link of the proposed inverter. Therefore, a level of $0.5V_{dc}$ is generated, which provides the capability for achieving more output levels in an expanded inverter. At the same time, the reduction in the step voltage makes the output voltage waveform of the proposed inverter closer to a sine wave, which is beneficial to improve the quality of the output waveform and reduce TSV. To achieve the same voltage gain, the DC source of the proposed inverter has to be doubled in relation to the others.

In addition, the advantages of using less switches in the proposed inverter are more prominent in the expanded topology. The output levels of the proposed inverter are twice those of other topologies under the same conditions. Therefore, a gain that is comparable to other inverters can be achieved. The comparisons of the expansion are shown in Figure 12, where m is the output level of the half cycle. In fact, m is discrete and limited to certain values; for intuitiveness, the results are presented in the form of continuous curves.

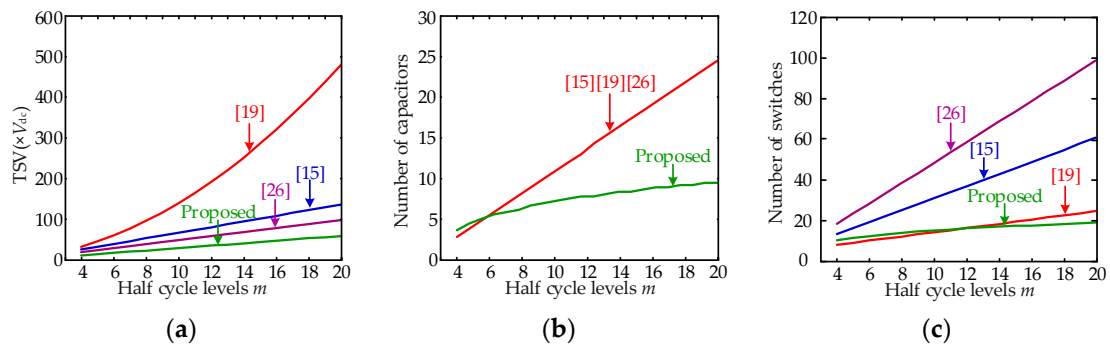


Figure 12. Comparison of expansions. (a) Total standing voltage (TSV). (b) Number of capacitors. (c) Number of switches.

It can be seen from Figure 12 that the proposed topology shows advantages for each comparison item. Only in some values of m are the number of switches higher than in the inverter proposed in [19]. However, the inverter in [19] uses a large number of diodes and does not have the ability to integrate inductive loads.

5. Simulation and Experiment Results

5.1. Simulation Results

The proposed topology was simulated in MATLAB/SIMULINK to verify the correctness of the theoretical analysis of the nine-level and seventeen-level inverters. Simulations were carried out under the condition that the input voltage was 30 V and the load was 30 Ω and 15 mH. The output voltages and currents of the two showcases are shown in Figures 13 and 14; Figure 15 shows the THD of the two inverters.

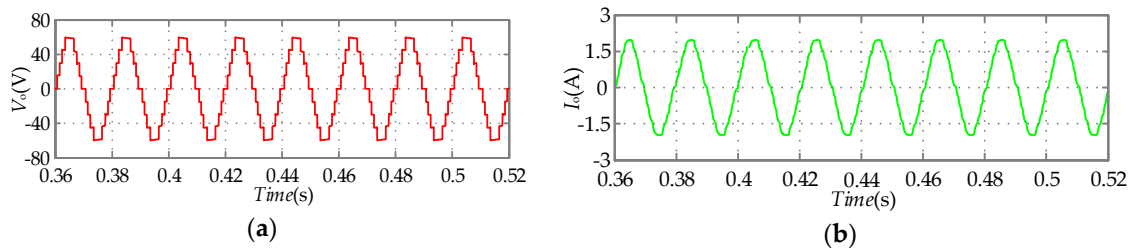


Figure 13. Waveforms of the nine-level inverter. (a) Voltage; (b) current.

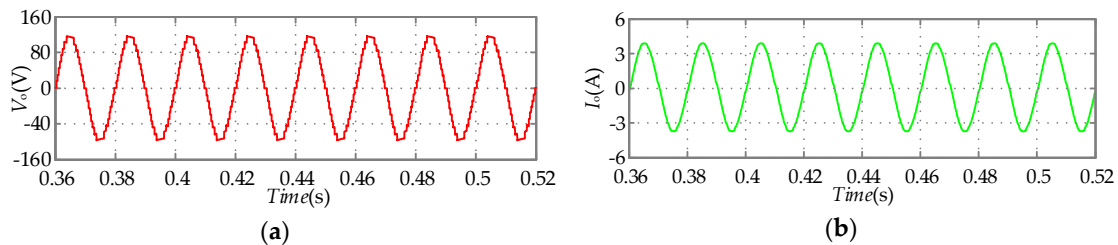


Figure 14. Waveforms of the seventeen-level inverter. (a) Voltage; (b) current.

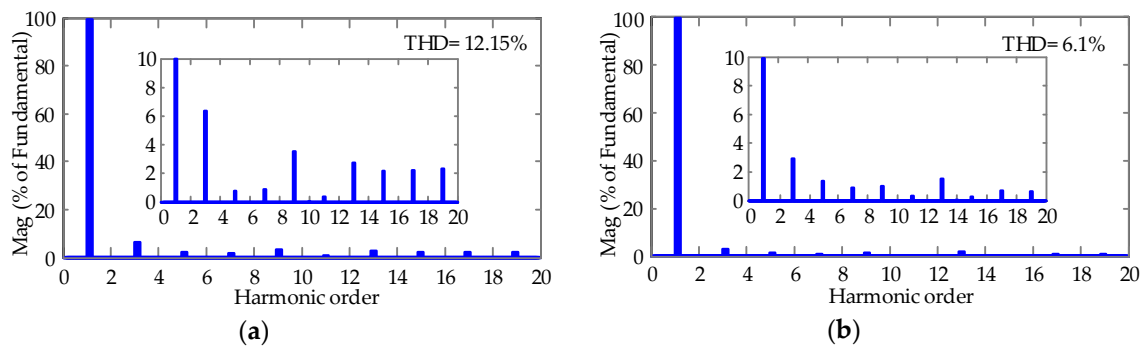


Figure 15. THD of two inverters. (a) THD of the nine-level inverter. (b) THD of the seventeen-level inverter.

It can be seen from the above results that the proposed inverter can achieve twice the voltage gain, and the seventeen-level waveform is closer to a sine wave. More levels can reduce the output voltage THD. The nine-level waveform has a THD of 12.15% and the THD of the seventeen-level waveform of a two-cascaded module is 6.1%.

5.2. Experiment Results

Experiments are implemented in this part to validate the dynamic and steady-state performance of the proposed nine-level inverter. The experimental parameters are shown in Table 6 and, the experimental platform is shown in Figure 16.

Table 6. Experimental parameters.

Parameters	Value
DC source	30 V
Capacitors	2200 μ F
R-load	100 Ω
L-load	60 mH
RL-load	30 Ω and 15 mH
Output frequency f_o	50 Hz
Switches (MOSFET)	SPP20N60C3
Optocoupler-driver	TLP250
Current probe	Tektronix A622

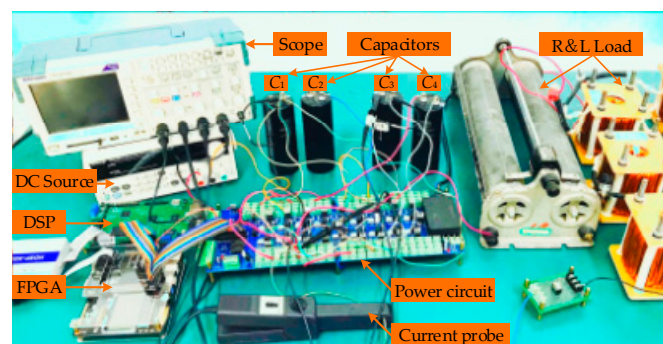


Figure 16. The experimental platform.

5.2.1. Steady-State Responses

Figure 17 shows the experimental results under the RL-load condition. It can be seen from Figure 17a that the voltage is a stable nine-level staircase wave with a peak value of 60 V at an input voltage of 30 V. A double voltage gain is obtained. The current lags behind the voltage by about 9° .

The voltages of capacitors are shown in Figure 17b. The voltages of C_2 and C_3 are maintained at 15 V by voltage self-balancing. The voltages of C_3 and C_4 are maintained at 30 V with a low voltage ripple of 9%. In addition, it can be seen from Figure 17b that C_1 and C_2 work in a symmetrical state and C_3 and C_4 work in a symmetrical state, which is consistent with the above analysis.

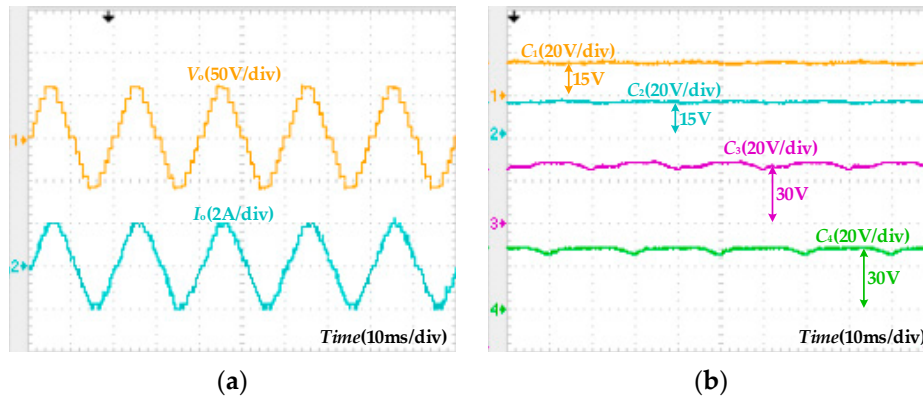


Figure 17. Experimental waveforms. (a) Output voltage and current. (b) Capacitor voltages.

The ability of integrating the pure inductive load of the proposed inverter is validated by conducting the L -load. The experimental results are shown in Figure 18. The current lags behind the voltage by 90° .

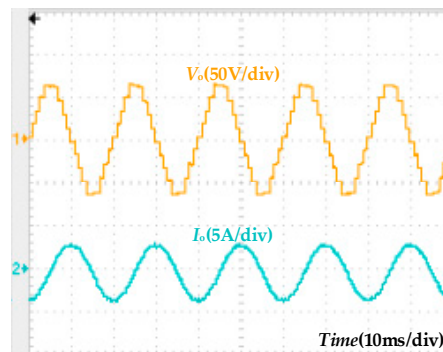


Figure 18. Output voltage and current under the L -load condition.

5.2.2. Dynamic Responses

The dynamic performance of the proposed inverter is validated in this section to emulate changes in the working status and parameters. Figure 19 shows the experimental results when the DC source is suddenly changed by switching to another DC source with a different voltage. Due to the symmetry of the capacitors, only two capacitor voltages are given. The output voltage and current, as well as the capacitor voltages, become stable quickly when the DC source is changed. The discharging of C_2 and C_3 are different because they work at different modes, as shown in Figure 19b.

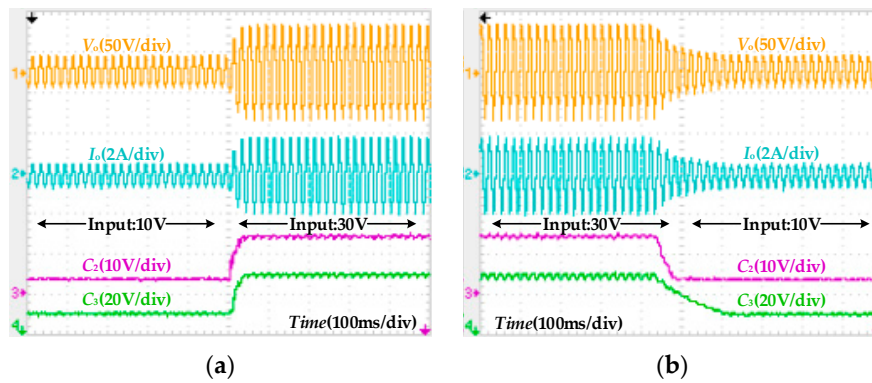


Figure 19. Experiment results when DC source changes. (a) Dc source changes from 10 V to 30 V. (b) Dc source change from 30 V to 10 V.

The experimental results when the load changes are shown in Figure 20, including from $R = \infty$ changes to RL -load, then changes to R -load. The dynamic performance of the inverter is excellent during the load changes, which indicates that the inverter can adapt to sudden changes and changes in load types.

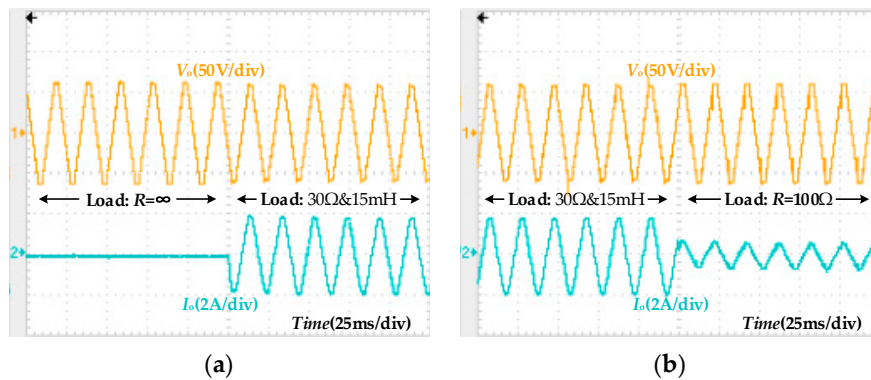


Figure 20. Experiment results when the load changes. (a) Load changes from $R = \infty$ to RL -load. (b) Load changes from RL -load to R -load.

The output frequency f_o is also a factor that may change during the operation of the inverter. The experiment is conducted under the condition that f_o changes from 50 Hz to 100 Hz and then changes from 50 Hz to 25 Hz. The outputs of the inverter are shown in Figure 21 when the output frequency changes. The experimental results show that the inverter can also quickly adapt to frequency changes.

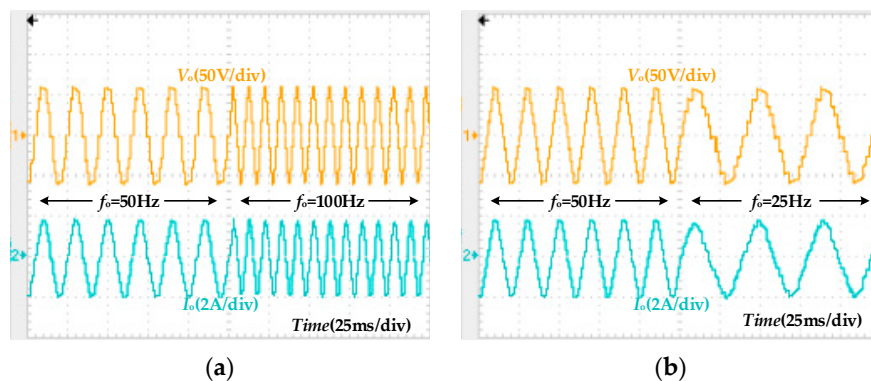


Figure 21. Experimental results when f_o changes. (a) f_o changes from 50 Hz to 100 Hz. (b) f_o changes from 50 Hz to 25 Hz.

5.2.3. Analysis of Losses

In Figure 17a, the root mean square values of output voltage and current are 41.02 V and 1.28 A. Based on the above analysis, the losses are caused by the capacitors, switches and diodes, which mainly relate to the parasitic parameters. The values of parasitic parameters are as follows: $V_D = 0.7$ V, $r_s = 5$ m Ω , $ESR_C = 60$ m Ω and $C_{ds} = 500$ pF. Incorporating the above parameters and experimental parameters into (17) to (20), the three types of losses can be obtained as: $P_{rip} = 0.89$ W, $P_{con} = 0.17$ W and $P_{sw} = 0.56$ W. The ratio between the three types of losses and the ratio between capacitors, switches and diodes (including body diode of the switch) are shown in Figure 22.

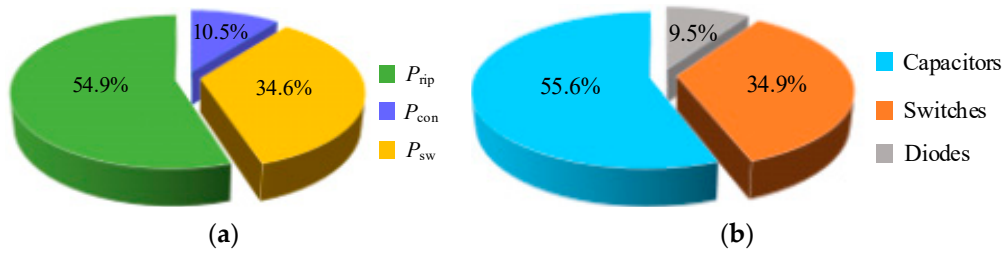


Figure 22. Losses distribution. (a) The ratio between the three types of losses. (b) The ratio between three types of devices.

The changes in the three types of losses when the output power increases are shown in Figure 23. P_{sw} increases in proportion to the output power, and the proportion of P_{con} tends to exceed the switching loss. The larger increase in P_{rip} is due to the corresponding increase in the voltage ripple of the capacitor when the output power increases.

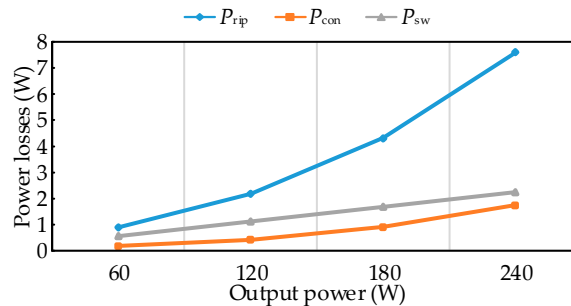


Figure 23. The variations of the three types of losses.

6. Conclusions

This paper presents a generalized multilevel inverter based on the T-type switched capacitor module (TSCM). The working principle and modulation strategy of the proposed inverter were analyzed with a nine-level inverter as an example. The symmetrical working state of the positive and negative half cycles of the voltage-dividing capacitors ensures voltage self-balancing. The step-by-step charging method of the switched capacitors and the modular expansion of the proposed inverter can effectively increase the output voltage levels and voltage gain.

The comparisons with other existing topologies show that the proposed inverter can reduce the number of devices, thereby reducing the capital cost and power losses. Moreover, the number of switches and capacitors of the proposed inverter grow in a logarithmic curve with the increase in the output voltage levels. In other words, our method is more prominent than other topologies in terms of the devices used when the output voltage levels are high. The modular expansion method makes the inverter easy to miniaturize, which brings convenience to practical applications.

A prototype has been built to validate the steady-state and dynamic performance of the proposed inverter. The experimental results show that the inverter has an excellent performance, indicating its broad application prospects in distributed power generation, such as photovoltaic power generation.

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Abbreviations

V_o	Output voltage
V_{dc}	Voltage of DC source
V_D	Voltage drop of diode
V_{eq}	Equivalent voltage on the load
V_k	K-th harmonic of voltage
V_s	Voltage stress of the switch
V_{oi}	Rectangular wave number i
C_i	Capacitor number i
$C_{i\ min}$	Minimum capacitance
C_{ds}	Parasitic capacitance of the switch
$\Delta V_{C2_0.5}$	Voltage ripple of C_2 when output $0.5V_{dc}$
$\Delta V_{C2_1.5}$	Voltage ripple of C_2 when output $1.5V_{dc}$
ΔV_{C3}	Voltage ripple of C_3
ΔQ_{C3}	Discharge amount of C_3 in one cycle
$\Delta Q_{C2_0.5}$	Discharge amount of C_2 when output $0.5V_{dc}$
$\Delta Q_{C2_1.5}$	Discharge amount of C_2 when output $1.5V_{dc}$
P_{rip}	Ripple losses
P_{con}	Conduction losses
P_{sw}	Switching losses
P_o	Output power
S_i	Switch number i
D_i	Diode number i
α_i	Conduct angle of rectangular wave
ω	Fundamental angular frequency
N	Output levels
G	Voltage gain
M	Fundamental wave modulation index
R	Load
f_o	Fundamental frequency
r_D	Internal resistance of diode
ESR_C	Equivalent resistance of the capacitor
r_s	Equivalent resistance of the switch
i_o	Output current
r_{eq}	Equivalent conducting resistance
f_s	Operating frequency of the switch
η	Efficiency of the nine-level inverter
m	Step number of half cycle
TSV	Total standing voltage
THD	Total harmonic distortion

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